Introduction to CMOS VLSI Design

Lecture 15: Nonideal Transistors

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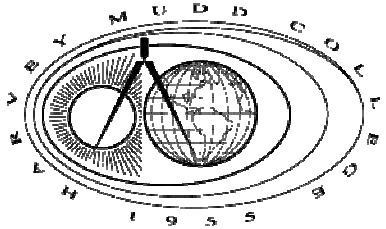

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Outline

- Transistor I-V Review
- Nonideal Transistor Behavior
  - Velocity Saturation
  - Channel Length Modulation
  - Body Effect
  - Leakage
  - Temperature Sensitivity
- Process and Environmental Variations
  - Process Corners

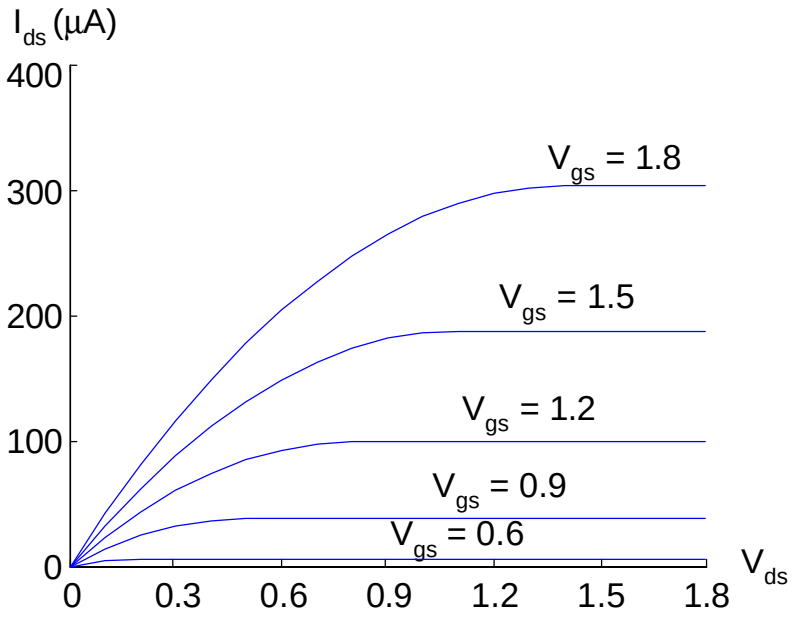
Ideal Transistor I-V

- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ b\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{b}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

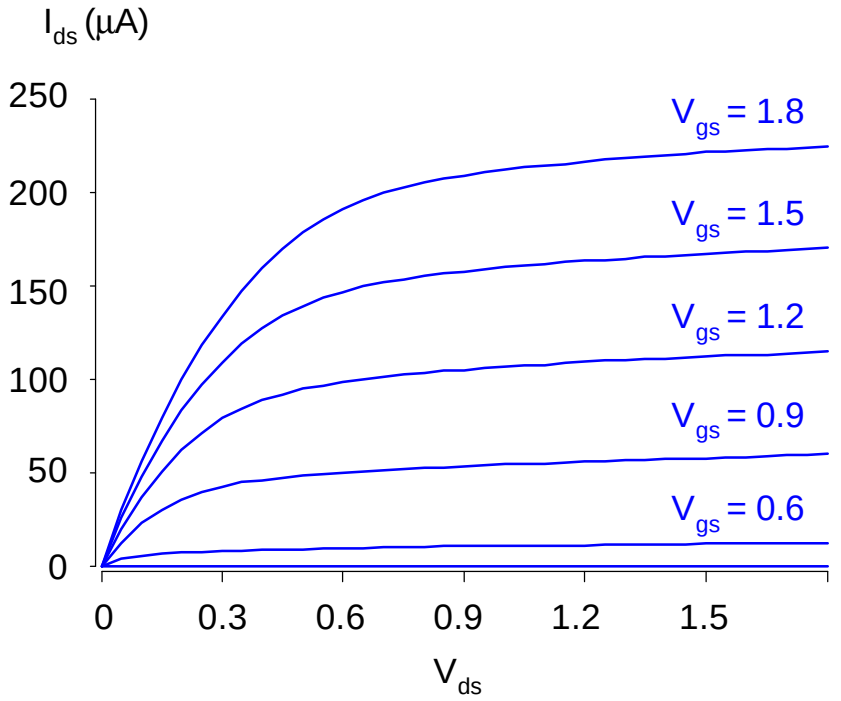
Ideal nMOS I-V Plot

- 180 nm TSMC process
- Ideal Models
  - $\beta = 155(W/L)\ \mu A/V^2$
  - $V_t = 0.4$ V
  - $V_{DD} = 1.8$ V



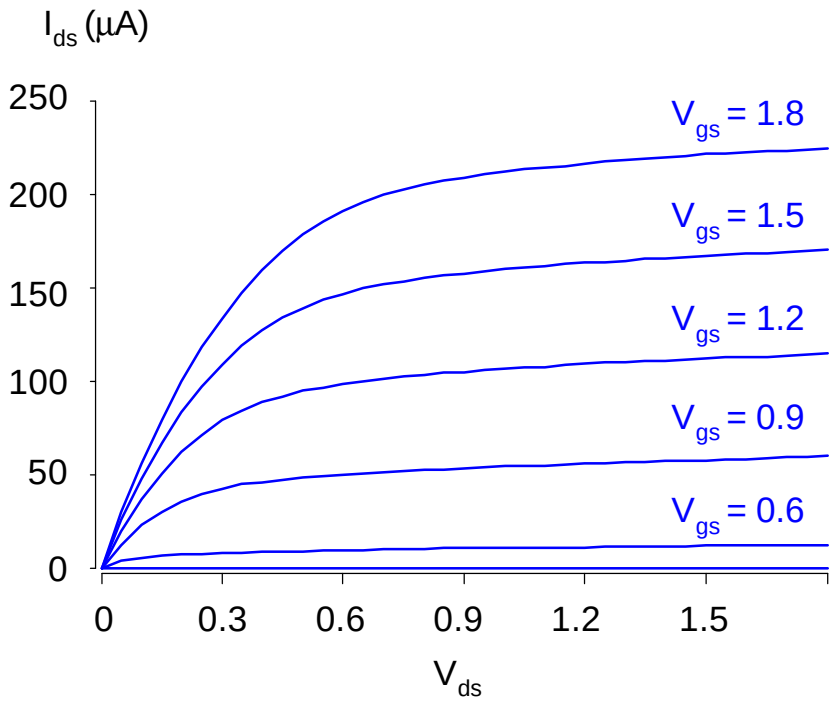
Simulated nMOS I-V Plot

- 180 nm TSMC process
- BSIM 3v3 SPICE models
- What differs?



Simulated nMOS I-V Plot

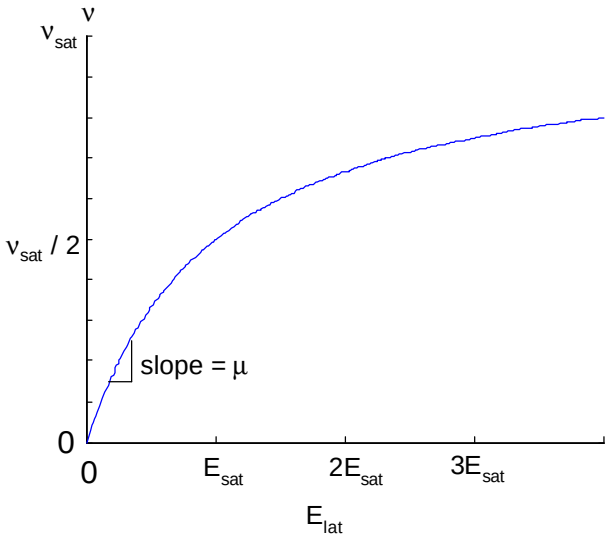
- 180 nm TSMC process
- BSIM 3v3 SPICE models
- What differs?
  - Less ON current
  - No square law
  - Current increases in saturation



Velocity Saturation

- We assumed carrier velocity is proportional to E-field
  - $v = \mu E_{lat} = \mu V_{ds}/L$
- At high fields, this ceases to be true
  - Carriers scatter off atoms
  - Velocity reaches v_{sat}
    - Electrons: 6-10 x 10^6 cm/s
    - Holes: 4-8 x 10^6 cm/s
  - Better model

$$v = \frac{\mu E_{lat}}{1 + \frac{E_{lat}}{E_{sat}}} \Rightarrow v_{sat} = \mu E_{sat}$$



Vel Sat I-V Effects

- Ideal transistor ON current increases with V_{DD}^2

$$I_{ds} = mC_{ox}\frac{W}{L}\frac{\left(V_{gs}-V_t\right)^2}{2} = \frac{b}{2}\left(V_{gs}-V_t\right)^2$$

- Velocity-saturated ON current increases with V_{DD}

$$I_{ds} = C_{ox}W\left(V_{gs}-V_t\right)v_{max}$$

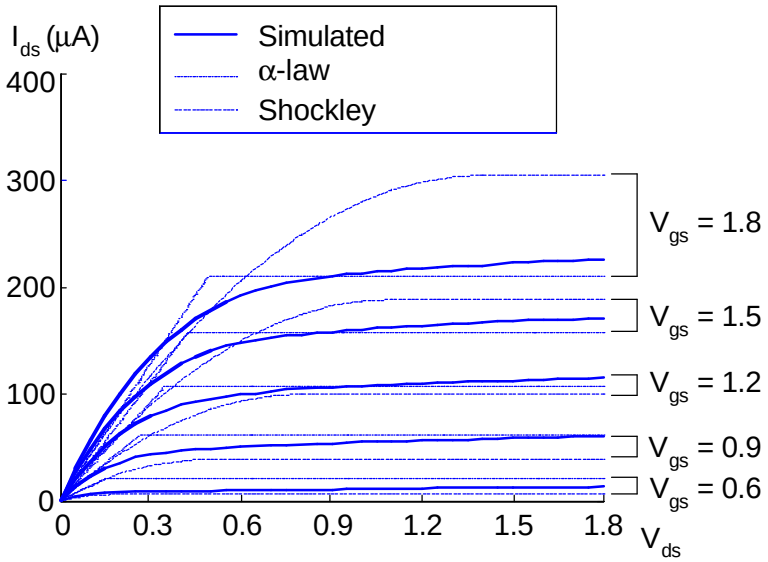
- Real transistors are partially velocity saturated
  - Approximate with α-power law model
  - $I_{ds} \propto V_{DD}^{\alpha}$
  - $1 < \alpha < 2$ determined empirically

α-Power Model

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ I_{dsat}\dfrac{V_{ds}}{V_{dsat}} & V_{ds} < V_{dsat} \quad \text{linear} \\ I_{dsat} & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

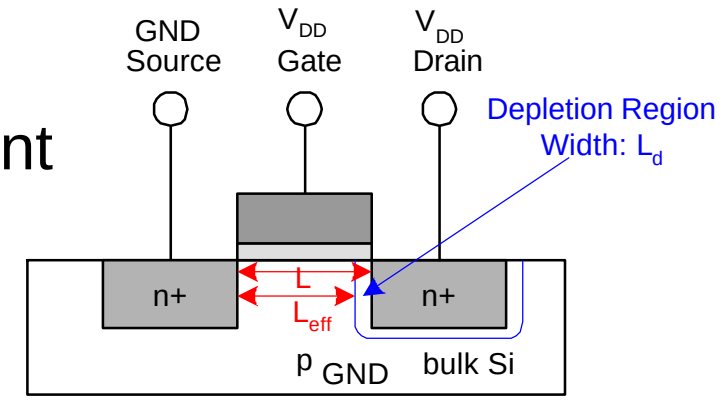
$$I_{dsat} = P_c \frac{b}{2}\left(V_{gs} - V_t\right)^a$$

$$V_{dsat} = P_v \left(V_{gs} - V_t\right)^{a/2}$$



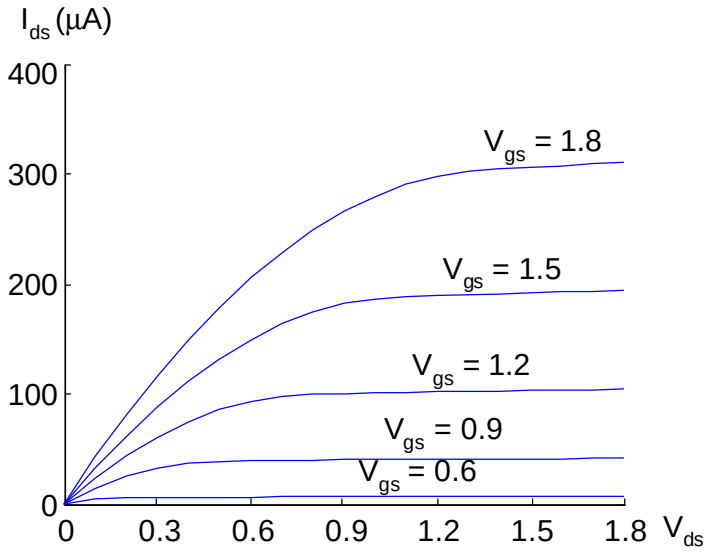
Channel Length Modulation

- Reverse-biased p-n junctions form a *depletion region*
  - Region between n and p with no carriers
  - Width of depletion L_d region grows with reverse bias
  - $L_{eff} = L - L_d$
- Shorter L_{eff} gives more current
  - I_{ds} increases with V_{ds}
  - Even in saturation



Chan Length Mod I-V

$$I_{ds} = \frac{b}{2}\left(V_{gs} - V_t\right)^2 \left(1 + l V_{ds}\right)$$



- λ = *channel length modulation coefficient*
  - not feature size
  - Empirically fit to I-V characteristics

Body Effect

- V_t: gate voltage necessary to invert channel
- Increases if source voltage increases because source is connected to the channel
- Increase in V_t with V_s is called the *body effect*

Body Effect Model

$$V_t = V_{t0} + g\left(\sqrt{f_s + V_{sb}} - \sqrt{f_s}\right)$$

- ϕ_s = *surface potential* at threshold

$$f_s = 2v_T \ln\frac{N_A}{n_i}$$

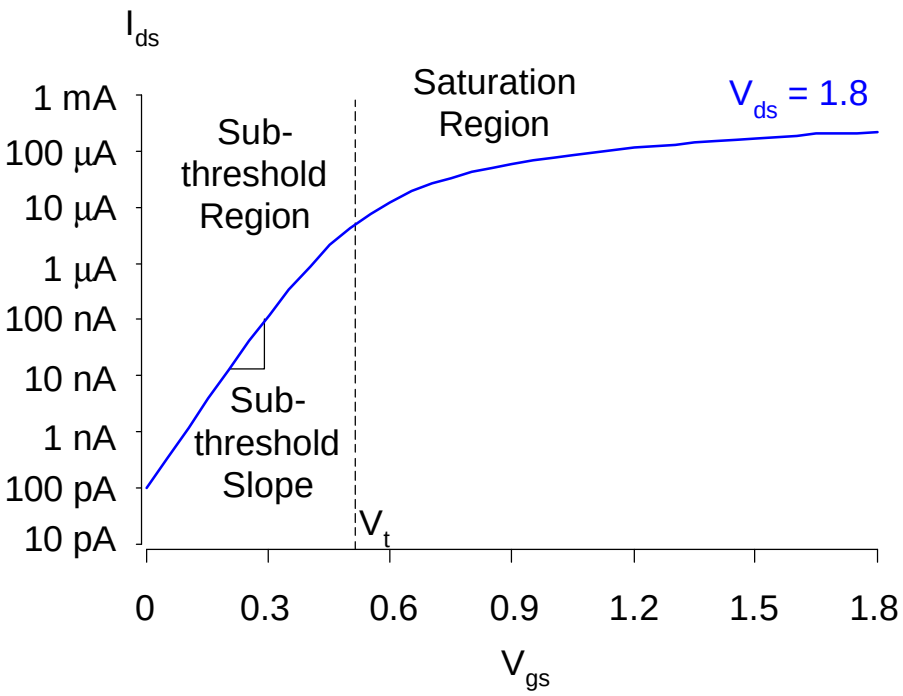
  - Depends on doping level N_A
  - And intrinsic carrier concentration n_i

- γ = *body effect coefficient*

$$g = \frac{t_{ox}}{e_{ox}}\sqrt{2qe_{si}N_A} = \frac{\sqrt{2qe_{si}N_A}}{C_{ox}}$$

OFF Transistor Behavior

- What about current in cutoff?
- Simulated results
- What differs?
  - Current doesn't go to 0 in cutoff



Leakage Sources

- Subthreshold conduction
  - Transistors can't abruptly turn ON or OFF
- Junction leakage
  - Reverse-biased PN junction diode current
- Gate leakage
  - Tunneling through ultrathin gate dielectric

- Subthreshold leakage is the biggest source in modern transistors

Subthreshold Leakage

- Subthreshold leakage exponential with V_{gs}

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_t}{n v_T}} \left(1 - e^{\frac{-V_{ds}}{v_T}} \right) \qquad I_{ds0} = b v_T^2 e^{1.8}$$

- n is process dependent, typically 1.4-1.5

DIBL

- Drain-Induced Barrier Lowering
  - Drain voltage also affect Vt

$$V_t' = V_t - \eta V_{ds}$$

  - High drain voltage causes subthreshold leakage to _____.

DIBL

- Drain-Induced Barrier Lowering
  - Drain voltage also affect V_t

$$V_t' = V_t - hV_{ds}$$

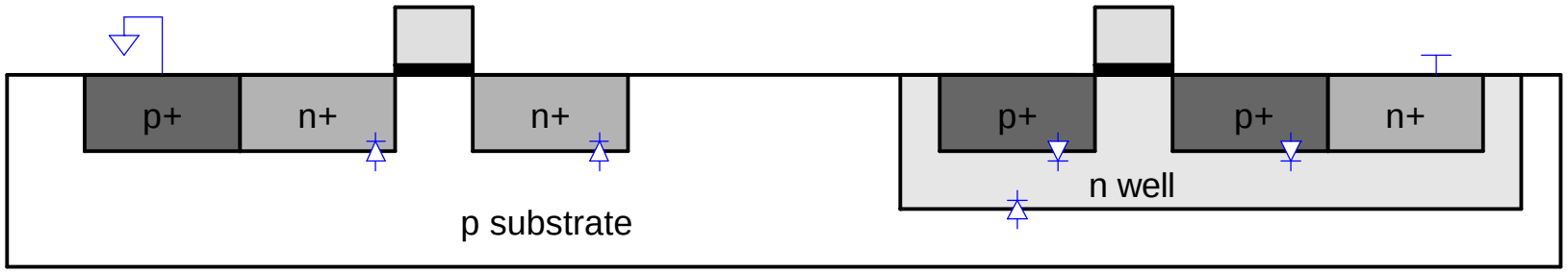
  - High drain voltage causes subthreshold leakage to increase.

Junction Leakage

- Reverse-biased p-n junctions have some leakage

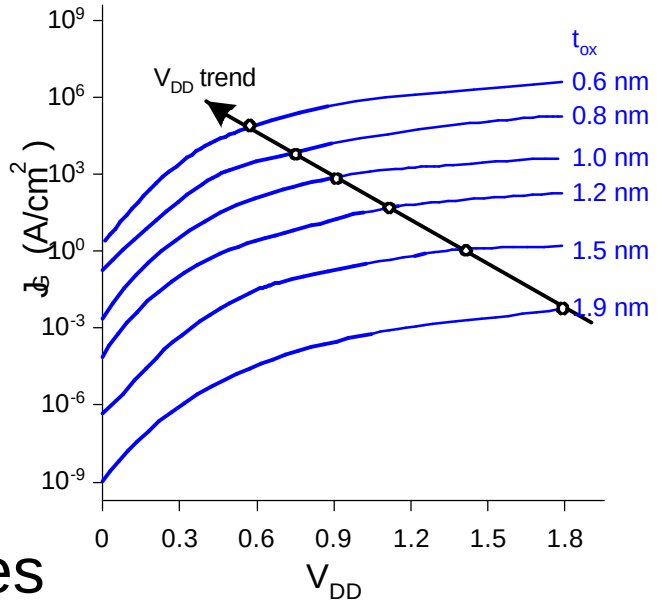
$$I_D = I_S\left(e^{\frac{V_D}{v_T}} - 1\right)$$

- I_s depends on doping levels
  - And area and perimeter of diffusion regions
  - Typically < 1 fA/μm^2



Gate Leakage

- Carriers may tunnel thorough very thin gate oxides
- Predicted tunneling current (from [Song01])



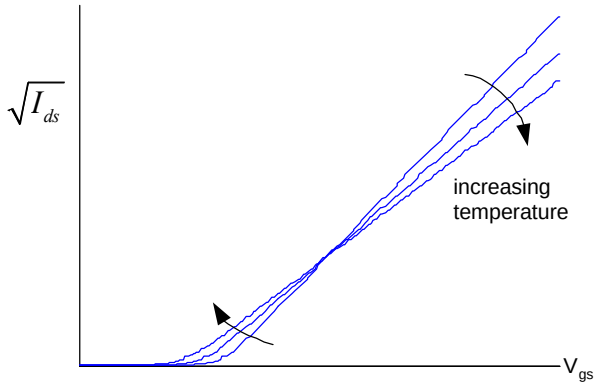
- Negligible for older processes
- May soon be critically important

Temperature Sensitivity

- Increasing temperature
  - Reduces mobility
  - Reduces V_t
- I_{ON} _____ with temperature
- I_{OFF} _____ with temperature

Temperature Sensitivity

- Increasing temperature
  - Reduces mobility
  - Reduces V_t
- I_{ON} decreases with temperature
- I_{OFF} increases with temperature

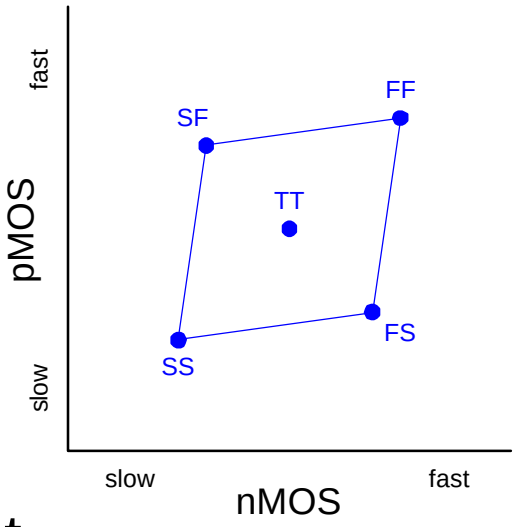


So What?

- So what if transistors are not ideal?
  - They still behave like switches.
- But these effects matter for…
  - Supply voltage choice
  - Logical effort
  - Quiescent power consumption
  - Pass transistors
  - Temperature of operation

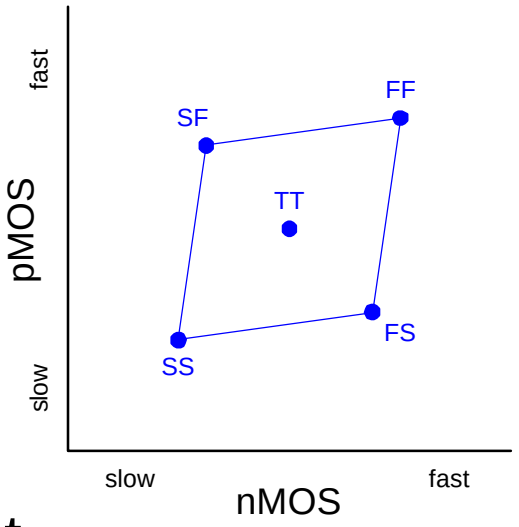
Parameter Variation

- Transistors have uncertainty in parameters
  - Process: L_{eff}, V_t, t_{ox} of nMOS and pMOS
  - Vary around typical (T) values
- Fast (F)
  - L_{eff}: _____
  - V_t: _____
  - t_{ox}: _____
- Slow (S): opposite
- Not all parameters are independent for nMOS and pMOS



Parameter Variation

- Transistors have uncertainty in parameters
  - Process: L_{eff}, V_t, t_{ox} of nMOS and pMOS
  - Vary around typical (T) values
- Fast (F)
  - L_{eff}: short
  - V_t: low
  - t_{ox}: thin
- Slow (S): opposite
- Not all parameters are independent for nMOS and pMOS



Environmental Variation

- V_{DD} and T also vary in time and space
- Fast:
  - V_{DD}: ____
  - T: ____

Corner	Voltage	Temperature
F		
T	1.8	70 C
S		

Environmental Variation

- V_{DD} and T also vary in time and space
- Fast:
  - V_{DD}: high
  - T: low

Corner	Voltage	Temperature
F	1.98	0 C
T	1.8	70 C
S	1.62	125 C

Process Corners

- Process corners describe worst case variations
  - If a design works in all corners, it will probably work for any variation.
- Describe corner with four letters (T, F, S)
  - nMOS speed
  - pMOS speed
  - Voltage
  - Temperature

Important Corners

- Some critical simulation corners include

Purpose	nMOS	pMOS	V_{DD}	Temp
Cycle time				
Power				
Subthrehold leakage				
Pseudo-nMOS				

Important Corners

- Some critical simulation corners include

Purpose	nMOS	pMOS	V_{DD}	Temp
Cycle time	S	S	S	S
Power	F	F	F	F
Subthrehold leakage	F	F	F	S
Pseudo-nMOS	S	F	?	?