Harris

Introduction to CMOS VLSI Design (E158)

Syllabus

Spring 2005

Teaching Staff

Professor: David Harris Parsons 2374 x73623 David_Harris@hmc.edu

Schedule

Lecture: MW 2:45-4:00
Office Hours: TBD

I am in my office more often than not, so feel free to stop by even if I do not have official office hours.

Texts

Weste & Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 3rd ed, Addison Wesley, 2005.
Patterson & Hennessy, *Computer Organization & Design*, 2nd ed, Morgan Kaufmann, 1998.

CMOS VLSI Design is the primary text. I recently completed the 3rd edition and am paying a bounty for each bug that is found. I would appreciate constructive criticism to help plan the 4th edition. *Computer Organization and Design* is the E85 textbook. You will be building a MIPS processor in this class following the design in the book, so it is assumed that you have access to the book and are familiar with the MIPS assembly language from Chapter 3, ALU design from Chapter 4, and the multicycle processor microarchitecture from Chapter 5, as well as combinational logic design and finite state machine design from Appendix B. Consider this knowledge a prerequisite to the class and get yourself up to speed if you feel rusty.

Electronic Communication

Class web page: http://www3.hmc.edu/~harris/class/e158
Class email list: eng-158-l

Be sure to check that you are on the class email list. You should have received email before the beginning of classes. If you did not receive mail, add yourself to the list or risk missing important late-breaking announcements. To subscribe, send email to listkeeper@hmc.edu with one line in the body:

subscribe eng-158-l

Grading

Labs:	40%
Final Project:	45%
Problem Sets:	10%
In-class Activities:	5%

The emphasis of this class is hands-on chip design. During the first six weeks, you will complete a series of labs to build your own MIPS microprocessor. Along the way, you will master a variety of CAD tools and design techniques. Based on this experience, you and a partner will propose and carry out a final project of your choosing. Projects that are fully verified may be eligible to be manufactured.

As you will discover, hands-on design is extraordinarily time-intensive. It is impossible for you to apply all the knowledge you gain from this class to an actual design, so a series of problem sets will give you an opportunity to master these concepts.

Labs and problem sets are due by the end of class and will not be graded if submitted late because solutions will be given out. However, the labs build toward assembly of the entire processor in Lab 5, so it is important not to fall behind. Your lowest lab and homework score and lowest two activities will be dropped before the average is calculated. You are welcome to discuss labs and problem sets with other students or with the instructor **after** you have made an effort by yourself. However, you must turn in your own work, not work identical to that of another student. Be sure to credit at the top of your assignment anyone with whom you discussed ideas. **It is an honor code violation to simply copy someone else's work or refer to solutions from previous years.**

Tentative Schedule

The attached schedule is a tentative plan that may change during the semester. The deadlines, however, are fixed unless otherwise notified; *do not assume* that they will change just because the lecture schedule changes.

The schedule lists reading associated with each lecture. You are expected to do the reading before class and be prepared to discuss it. However, you may skip over advanced sections marked with a black square.

00000	19-Jan	Introduction and overview	1.1-1.4	
00001	24-Jan	Circuits, fabrication, and layout	1.5	
00010	26-Jan	Microprocessor example	1.6-1.12	Lab 1 due
00011	31-Jan	CMOS transistor theory	2.1-2.3	PS 1 due
00100	2-Feb	DC and transient response	2.5-6, 4.1-4.2	Lab 2 due
00101	7-Feb	Logical effort	4.3	PS 2 due
00110	9-Feb	-- Silicon Run Video --	3.1-3.8 (skim)	Lab 3 due
	14-Feb	Interconnect engineering	4.5-4.6	PS 3 due
00111	16-Feb	Simulation	5.1-5.3	Lab 4 due
01000	21-Feb	Combinational circuit design	6.1-6.2.1	Preliminary prop due
01001	23-Feb	Circuit families	6.2.2-6.2.5	Lab 5
01010	28-Feb	Sequential circuit design	7.1-7.3.6	Project proposal due
01011	2-Mar	Adders	10.1-10.2	PS 4 due
01100	7-Mar	Datapath functional units	10.3-10.9	
01101	9-Mar	TBD		Floorplan due
	14-Mar	-- Spring Break: No Class --		
	16-Mar	-- Spring Break: No Class --		
01110	21-Mar	Memories	11.1-11.2	
01111	23-Mar	Memories	11.5-11.7	Schematics complete
10000	28-Mar	Non-ideal transistor characteristics	2.4	PS 5 due
10001	30-Mar	Low power guest lecture: Dr. Ram Krishnamurthy	4.4, 6.5	
10010	4-Apr	In-class design reviews		Leaf cells complete
10011	6-Apr	In-class design reviews		
10100	11-Apr	Design margining and circuit pitfalls	4.7-4.8, 6.3	
10101	13-Apr	Design for testability	9.1-9.7 (skim)	Final Project due
10110	18-Apr	Skew-tolerant circuit design	7.5.1-7.5.2	
10111	20-Apr	Packaging, I/O, & clock and power distribution	12.1-12.5	PS 6 due
11000	25-Apr	Scaling and economics	4.9, 8.5	
11001	27-Apr	A History of Intel Microprocessor Chips	4.10-4.11	

Note: Final project presentations will take place during presentation days (May 4).

Upon completion of E158, the successful student will be able to:

1. Use the Electric CAD tool to build an 8-bit MIPS microprocessor including
    a. Schematic entry
    b. Layout
    c. Transistor-level cell design
    d. Gate-level logic design
    e. Hierarchical design
    f. Switch-level simulation (IRSIM)
    g. Design rule checking (DRC)
    h. Electrical rule checking (ERC)
    i. Network consistency checking (NCC)
    j. HDL design (Verilog)
    k. Logic synthesis (Synopsys Design Analyzer)
    l. Place and route
    m. Pad frame generation and routing
    n. Pretapeout verification
2. Design one's own custom integrated circuit from concept through tapeout including
    a. Team design skills and partitioning
    b. Specification
    c. Logic design
    d. Circuit design
    e. Floorplanning and physical design
    f. Design verification
    g. Tapeout
3. Estimate and optimize combinational circuit delay using RC delay models and logical effort
4. Simulate circuits with HSPICE and tune for performance
5. Estimate and optimize interconnect delay and noise
6. Design for higher performance or lower area using alternative circuit families
7. Describe and avoid common CMOS circuit pitfalls and reliability problems
8. Compare the tradeoffs of sequencing elements including flip-flops, transparent latches, and pulsed latches
9. Design functional units including adders, multipliers, ROMs, SRAMs, and PLAs
10. Describe the sources and effects of clock skew
11. Predict the capabilities of future CMOS processes using scaling theory and the SIA roadmap
12. Evaluate the economics of integrated circuit design