E158 Final Project Grading Sheet

Project:

Designers:

Checkoff

Proposed Project Difficulty	____	/ 10
Project Meets Specifications	____	/ 5
Schematic Quality	____	/ 4
Layout Quality	____	/ 4
Implementation		
Project In Pad Frame	____	/ 2
DRC	____	/ 2
ERC	____	/ 2
NCC	____	/ 5
Test Cases	____	/ 5
Simulation	____	/ 2
Total	**____**	**/ 41**

Final Report

Color Chip Plot   ____ / 1
    attractive and legible

Functional Overview   ____ / 3
    clear to other engineers

Chip Pinout   ____ / 1
    padframe labeled with pin names,
        input/output/bidir

Chip Floorplan   ____ / 2
    captions and dimensions of final
    design, relation to original floorplan,
    explanation of discrepancies

Area and Design Time Data   ____ / 3
    table listing area and design time
    for each cell in the design

Simulation Results   ____ / 5
    description of simulations performed
    include a few pages of key waveforms
    convince reader design works
    estimate maximum operating speed

Verification Results   ____ / 1
    DRC, ERC, NCC pass

Schematics / Verilog   ____ / 2
    complete set of drawn schematics
    and Verilog for synthesized blocks
    legible and well-commented

Layout   ____ / 2
    complete set of color layout
    clean and efficient

Writing quality   ____ / 9
    Clarity, organization, grammar, brevity

Project linked to web page
    report submitted in PDF form   ____ / 1
    CIF & all libraries submitted   ____ / 1
    IRSIM .cmd file submitted   ____ / 1

International collaboration (if applicable)   ____ / *3*
    communication methods used
    reflections on project

Total   **____ / 32-35**